REMARKS

Claims 1, 3-17, and 19-22 were pending in the Office Action. Applicants have amended Claims 6, 7, 9, 17, and 19. Applicants respectfully request reconsideration and reexamination of the application.

Claims 1, 3-17, and 19-22 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner cites Claim 7 as not reciting functions of the alias register and the alias link pointer lp (OA, p. 2). To clarify Claim 7, Applicants have amended Claim 7 to recite "the address of the instruction word following the instruction word begun with the call instruction is held in an alias register, an implicit operand of the call instruction, with an assembler using an alias link pointer lp for pointing to the alias register." No new matter has been added and support for the amendment can be found, for example, on page 24 line 23 through page 25 line 9.

Examiner cites Claim 19 as being unclear as to "the register file generating two pointers" (OA, p. 2). To clarify Claim 19, Applicants have amended Claim 19 to recite "wherein a register read of the explicitly-specified register is accompanied by a register read of the implicitly-derived register when implicit derivation of a register specifier is selected." No new matter has been added and support for the amendment can be found, for example, on page 18 lines 16-21.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Examiner cites, as examples, Claims 1, 3, 21, and 22 and states the proposition that a "decoder is commonly for decoding opcodes or for generating control signals in response to opcodes and not for deriving anything as recited in the claims" (OA, p. 2). Applicants

respectfully disagree and submit that the claims are fully supported by the specification. For example, Applicants refer Examiner to Figs. 5A, 6, and 9, along with the accompanying text for a discussion of certain embodiments of a decoder in accordance with the present invention. As a specific example of an embodiment, a read circuit is disclosed in Fig. 9 that may be implemented within a decoder to generate implicitly-derived register specifiers (p. 20, lns. 3-21).

Examiner cites Claim 4 and notes that the claim is vague and indefinite because it is not clear how exactly the registers are addressed, by association or by addresses (OA, pp. 2-3). Applicants disagree and refer Examiner to, for example, Figs. 4 through 6 and accompanying text. As an example, even though functional units are associated with respective register file segments, each register file segment may have a number of registers that are addressable (p. 17, lns. 1-12).

Examiner cites Claim 6 as being unclear regarding register rs2 and rd. Applicants have amended Claim 6 to clarify that register rs2 contains data that describes the extracted field of registers r[rs1] and r[rs1+1] and that register r[rd] is the destination register.

Examiner cites Claim 9 for having a space missing between two words. Applicants have amended the claim to correct the typographical error.

Examiner cites Claim 17 for the decoder function being unclear and suggesting the insertion of "pointing" after the word "pointer." Applicants have amended Claim 17 as suggested by Examiner.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Examiner cites Claim 20 as vague and indefinite for the term "defining" in "defining a register specifier." Applicants respectfully disagree and believe that "explicitly defining a register specifier" as recited in Claim 20 is not vague and indefinite. The specification in

numerous places describes an explicitly defined register or register specifier. For example, on page 32 lines 17-18, there is described a first source register that is explicitly defined as r[rs1] and includes an implicitly-derived register specifier r[rs1+1]. The term "defined" or "defining" is clear from the text that it refers to the register or register specifier that is explicitly specified, in contrast to the register or register specifier that is implicitly derived.

Examiner requests Applicants to identify the portion of the specification which discloses how exactly Applicants' decoder implicitly derives a register specifier based on an explicitly-specified register specifier. Applicants refer Examiner to Figs. 5A, 6, and 9, along with the accompanying text for a discussion of certain embodiments of a decoder in accordance with the present invention. As a specific example of an embodiment, a read circuit is disclosed in Fig. 9 that may be implemented within a decoder to generate implicitly-derived register specifiers based on an explicitly-specified register specifier (p. 20, lns. 3-21).

Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 112, second paragraph, of Claims 1, 3-17, and 19-22 be withdrawn.

Claims 1, 3, 5-17, and 19-22 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 3,931,615 to Oliver et al. [herein referred to as "Oliver"] in view of U.S. Patent No. 3,833,904 to Gebhardt et al. [herein referred to as "Gebhardt"].

Examiner admits that Oliver fails to teach deriving the implicitly derived register specifier based on the explicitly-specified register specifier and attempts to cure the deficiency by combining Oliver with Gebhardt (OA, p. 4). However, Gebhardt simply discloses a program counter that "is incremented by one after an instruction is fetched from memory" (col. 36, lns. 38-41) and "provides the base for the operand address when the relative addressing option is employed" (col. 36, lns. 46-50). Consequently, neither Oliver

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MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

nor Gebhardt, alone or in combination, teach or suggest a "decoder implicitly deriving said implicitly derived register specifier based on said explicitly-specified register specifier of the instruction" as recited in Claim 1 or "implicitly deriving a register specifier based on the explicitly defined register specifier" as recited in Claim 20.

Examiner further cites Gebhardt as teaching "a processor having a plurality of functional units (col. 36 line 34)" (OA, p. 4). Applicants disagree because the functional units referred to, at col. 36, line 34, are within the processor 610 shown in block diagram in Fig. 13, which are the functional blocks that make up a processor, such as program counter 613, command register 614, buffer register 615, etc. (col. 36, ln. 34 to col. 39, ln. 63, and Fig. 13). In contrast, functional units in accordance with an embodiment of the present invention are, for example, processors, such as a digital signal processor or a RISC processor (p. 8, ln. 27 to p. 9, ln. 10).

Therefore, Applicants respectfully submit that Claims 1 and 20 patentably distinguish over Oliver in view of Gebhardt and that corresponding dependent Claims 3, 5-17, 19, 21, and 22 are also distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claims 1, 3, 5-17, and 19-22 be withdrawn.

Claim 4 was rejected under 35 U.S.C. § 103(a) as being obvious over Oliver and Gebhardt in view of U.S. Patent No. 6,311,261 to Chamdani et al. [herein referred to as "Chamdani"].

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Examiner cites Chamdani for disclosing a VLIW processor (OA, p. 5). However, Chamdani fails to cure the deficiencies noted above for Oliver and Gebhardt. Therefore, Applicants respectfully submit that Claim 1 patentably distinguishes over Oliver and

Gebhardt in view of Chamdani and that dependent Claim 4 is also distinguishable for at least the same reasons as for corresponding independent Claim 1. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claim 4 be withdrawn.

Accordingly, Applicants respectfully submit that Claims 1, 3-17, and 19-22 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited. If there are any questions regarding any aspect of the application, please call the undersigned at (949) 718-5221.

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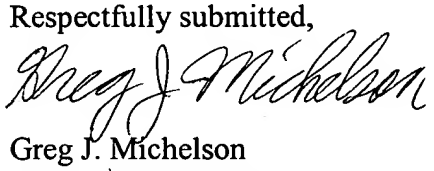
Respectfully submitted,



Greg J. Michelson
Attorney for Applicants
Reg. No. 44,940

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

ATTACHMENT A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the following, insertions are underlined and deletions are enclosed in **bold** brackets.

6. (Amended) A processor according to Claim 1 wherein:

the instruction is a bit extract instruction that uses an implicitly-derived register specifiers and has a form of:

bitext rsl, rs2, rd,

and performs an operation of extracting bits from even-aligned pairs of registers r[rsl] and [rsl+1] where the term [rsl+l] designates data contained within the register following the explicitly-defined register rsl, wherein data in register r[rs2] describes the extracted field of registers r[rs1] and r[rs1+1] and register r[rd] is a destination register.

7. (Amended) A processor according to Claim 1 wherein:

the instruction is a call instruction that uses an implicitly-derived register specifiers and has a form of:

call label,

causing a control transfer to an address specified by a label operand, the address of the instruction word following the instruction word begun with the call instruction is held in an alias register, an implicit operand of the call instruction, with an assembler using an alias link pointer lp for pointing to the alias register.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

9. (Amended) A processor according to Claim 1 wherein:

the instruction is a double-precision floating point compare instruction that uses an implicitly-derived register specifiers and has a form of:

dcmpcc rsl, rs2, rd,

and performs an operation of comparing data in registers (rsl, [rsl+1]) with data in registers (rs2, [rs2+1]) and storing a result in registers (rd,[rd+l]) where the terms (rsl, [rsl+l]), (rs2, [rs2+1]), and (rd, [rd+1]) designate double-precision words, and cc designates a condition code including equal, less than, and less than or equal to conditions.

17. (Amended) A processor according to Claim 1 wherein said decoder is generating a first pointer pointing to the explicitly-specified register and a second pointer pointing to the implicitly-derived register.

19. (Amended) A processor according to Claim 1 further comprising:

a pointer coupled to the register file and designating a register in the register file, the pointer including a signal indicative of selection of a implicitly-derived register, wherein a register read of the explicitly-specified register is accompanied by a register read of the implicitly-derived register [the register file generating two pointers, one directed to the explicitly-specified register and a second directed to the implicitly-derived register] when implicit derivation of a register specifier is selected.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979